IN THE CLAIMS

1-46 (Canceled)

47. (Original) A method for forming an electronic packaging assembly, comprising:

forming a silicon interposer, wherein the interposer includes micro-machined vias formed through the silicon interposer;

attaching a number of flip chips to the silicon interposer, wherein the flip chips couple to the micro-machined vias; and

coupling a Peltier element to at least one of the flip chips.

48 (Original) The method of claim 47, wherein attaching a number of flip chips to the silicon interposer includes:

coupling a microprocessor chip to the silicon interposer; and

coupling a memory chip to the silicon interposer.

49. (Original) The method of claim 48, wherein coupling a memory chip to the silicon interposer includes coupling a dynamic random access memory (DRAM) chip to the silicon interposer.

50. (Original) The method of claim 48, wherein the method further includes coupling capacitor to the silicon interposer.

51. (Original) The method of claim 47, wherein coupling a Peltier element to at least one of the flip chips includes coupling a Copper (Cu) and p-type semiconductor junction to the flip chip.

52. (Original) The method of claim 51, wherein coupling a Copper (Cu) and p-type semiconductor junction to the flip chip includes coupling a p-type semiconductor selected from the group consisting of p-doped Bismuth Telluride (Bi_2Te_3), p-doped Lead Telluride (PbTe), and p-doped Silicon Germanium (SiGe).

53. (Original) The method of claim 47, wherein coupling a Peltier element to at least one of the flip chips includes coupling a Copper (Cu) and n-type semiconductor junction to the flip chip.

54. (Original) The method of claim 53, wherein coupling a Copper (Cu) and n-type semiconductor junction to the flip chip includes coupling an n-type semiconductor selected from the group consisting of n-doped Bismuth Telluride (Bi_3Te_2), n-doped Lead Telluride (PbTe), and n-doped Silicon Germanium (SiGe).

55. (Original) A method for packaging an integrated circuit, comprising:

providing a silicon interposer having opposing sides;

coupling a semiconductor chip to each of the opposing sides of the silicon interposer;

coupling the semiconductor chips on each side of the silicon interposer to one another through the silicon interposer by a number of micro-machined vias, wherein the micro-machined vias provide electrical connections between the opposing sides of the silicon interposer; and

coupling a Peltier element to at least one of the of the semiconductor chips.

56. (Original) The method of claim 55, wherein coupling the Peltier element to at least one of the semiconductor chips includes coupling a metal-to-semiconductor Peltier element, wherein the semiconductor includes either an n or p-doped semiconductor alloy formed between Antimony (Sb) and a transition metal (T) from Group VIII, including Cobalt, Rhodium, and Iridium (Co, Rh, and Ir), and wherein the alloy has the general formula Tsb_3.

57. (Original) The method of claim 55, wherein coupling the Peltier element to at least one of the semiconductor chips includes coupling a metal-to-semiconductor Peltier element, wherein the semiconductor includes either an n or p-doped superlattice comprising alternating layers of $(PbTeSe)_m$ and $(BiSb)_n$ where m and n are the number of PbTeSe and BiSb monolayers per superlattice period.

58. (Original) The method of claim 55, wherein coupling the Peltier element to at least one of the semiconductor chips includes coupling a metal-to-semiconductor Peltier element, wherein the semiconductor is a doped complex oxide.

59. (Original) The method of claim 55, wherein coupling the Peltier element to at least one of the semiconductor chips includes coupling a metal-to-semiconductor Peltier element, wherein the semiconductor is selected from the group consisting of n-doped Bismuth Telluride (Bi_2Te_3), n-doped Lead Telluride (PbTe), and n-doped Silicon Germanium (SiGe).

60. (Original) The method of claim 55, wherein coupling a semiconductor chip to each of the opposing sides of the silicon interposer includes attaching a microprocessor chip to the first side of the silicon interposer.

61. (Original) The method of claim 55, wherein coupling a semiconductor chip to each of the opposing sides of the silicon interposer includes attaching a DRAM chip to a second side of the silicon interposer.

62. (Original) A method for packaging an integrated circuit, comprising:

providing a silicon interposer having opposing sides;

coupling a semiconductor chip to each of the opposing sides of the silicon interposer;

coupling the semiconductor chips on each side of the silicon interposer to one another through the silicon interposer by a number of micro-machined vias, wherein the micro-machined vias provide electrical connections between the opposing sides of the silicon interposer;

coupling a metal-to-semiconductor junction to at least one of the of the semiconductor chips, wherein the semiconductor includes a doped complex oxide semiconductor.

63. (Original) The method of claim 62, wherein coupling a doped complex oxide semiconductor includes coupling an n-doped complex oxide semiconductor comprising Strontium (Sr) and Titanium (Ti).

64. (Original) The method of claim 62, wherein coupling a doped complex oxide semiconductor includes coupling an oxygen deficient n-doped complex oxide semiconductor.

65. (Original) A method for packaging an integrated circuit, comprising:

providing a silicon interposer having opposing sides;

coupling a semiconductor chip to each of the opposing sides of the silicon interposer;

coupling the semiconductor chips on each side of the silicon interposer to one another through the silicon interposer by a number of micro-machined vias, wherein the micro-machined vias provide electrical connections between the opposing sides of the silicon interposer;

coupling a metal-to-semiconductor junction to at least one of the semiconductor chips, wherein the semiconductor includes an n-doped superlattice comprising alternating layers of $(PbTeSe)_m$ and $(BiSb)_n$ where m and n are the number of PbTeSe and BiSb monolayers per superlattice period.

66. (Original) A method for packaging an integrated circuit, comprising:

providing a silicon interposer having opposing sides;

coupling a semiconductor chip to each of the opposing sides of the silicon interposer;

coupling the semiconductor chips on each side of the silicon interposer to one another through the silicon interposer by a number of micro-machined vias, wherein the micro-machined vias provide electrical connections between the opposing sides of the silicon interposer;

coupling a metal-to-semiconductor junction to at least one of the of the semiconductor chips, wherein the semiconductor includes either an n or p-doped semiconductor alloy formed between Antimony (Sb) and a transition metal (T) from Group VIII, including Cobalt, Rhodium, and Iridium (Co, Rh, and Ir), and wherein the alloy has the general formula TSb_3.

67. (Original) A method for cooling an integrated circuit, comprising:

providing a silicon interposer having opposing sides;

coupling a first semiconductor chip to a first side of the silicon interposer;

coupling a second semiconductor chip to a second side of the silicon interposer, wherein a number of electrical connections through the silicon interposer couple the first semiconductor chip to the second semiconductor;

forming a metal-to-semiconductor junction which couples to the first semiconductor chip on the first side of the silicon interposer; and

passing current through the metal-to-semiconductor junction in a direction such that a Peltier cooling effect occurs adjacent to the first semiconductor chip.

68. (Original) The method of claim 67, wherein coupling a first semiconductor chip to the first side of the silicon interposer includes coupling a microprocessor chip to the first side.

69. (Original) The method of claim 67, wherein coupling a second semiconductor chip to the second side of the silicon interposer includes coupling a memory chip to the second side of the silicon interposer.

70. (Original) The method of claim 67, wherein forming a metal-to-semiconductor junction includes forming a Copper (Cu) and doped Bismuth Telluride (Bi_2Te_3) junction.

71. (Original) The method of claim 70, wherein forming a forming a Copper (Cu) and doped Bismuth Telluride (Bi_2Te_3) junction includes using vacuum evaporation to form a thin film of p-doped Bismuth Telluride (Bi_2Te_3).

72. (Original) The method of claim 67, wherein forming a metal-to-semiconductor junction includes forming a Copper (Cu) and doped Antimony Telluride (Sb_2Te_3) junction, wherein forming a forming a Copper (Cu) and doped Antimony Telluride (Sb_2Te_3) junction includes using vacuum evaporation to form a thin film of doped Antimony Telluride (Sb_2Te_3).

73. (Original) The method of claim 67, wherein forming a metal-to-semiconductor junction includes forming a Copper (Cu) and doped semiconductor junction, wherein the semiconductor is selected from Bismuth Telluride (Bi_2Te_3), Lead Telluride (PbTe), and Silicon Germanium (SiGe).

74. (Original) The method of claim 67, wherein forming a metal-to-semiconductor junction includes forming a metal-to-semiconductor junction which includes a doped superlattice junction, wherein the doped superlattice includes alternating layers of $(PbTeSe)_m$ and $(BiSb)_n$ where m and n are the number of PbTeSe and BiSb monolayers per superlattice period.

75. (Original) The method of claim 67, wherein forming a metal-to-semiconductor junction includes forming a metal-to-semiconductor junction wherein the semiconductor includes a

complex oxide semiconductor, and wherein the complex oxide semiconductor includes Strontium (Sr) and Titanium (Ti).

76. (Original) A method for heating an integrated circuit, comprising:

providing a silicon interposer having opposing sides;

coupling a first semiconductor chip to a first side of the silicon interposer;

coupling a second semiconductor chip to a second side of the silicon interposer, wherein a number of electrical connections through the silicon interposer couple the first semiconductor chip to the second semiconductor;

forming a metal-to-semiconductor junction which couples to the first semiconductor chip on the first side of the silicon interposer; and

passing current through the metal-to-semiconductor junction in a direction such that a Peltier heating effect occurs adjacent to the first semiconductor chip.

77. (Original) The method of claim 76, wherein coupling a first semiconductor chip to the first side of the silicon interposer includes coupling a microprocessor chip to the first side.

78. (Original) The method of claim 76, wherein coupling a second semiconductor chip to the second side of the silicon interposer includes coupling a memory chip to the second side of the silicon interposer.

79. (Original) The method of claim 76, wherein forming a metal-to-semiconductor junction includes forming a metal-to doped semiconductor junction wherein the semiconductor is selected from Bismuth Telluride (Bi_2Te_3), Lead Telluride (PbTe), and Silicon Germanium (SiGe).

80. (Original) The method of claim 76, wherein forming a metal-to-semiconductor junction includes forming a metal and doped superlattice junction, wherein the doped superlattice includes alternating layers of $(PbTeSe)_m$ and $(BiSb)_n$ where m and n are the number of PbTeSe and BiSb monolayers per superlattice period.

81. (Original) The method of claim 76, wherein forming a metal-to-semiconductor junction includes forming a metal and doped complex oxide semiconductor, wherein the complex oxide semiconductor includes Strontium (Sr) and Titanium (Ti).

82. (Original) A method for cooling an integrated circuit, comprising:

providing a silicon interposer having opposing sides;

coupling a first semiconductor chip to a first side of the silicon interposer;

coupling a second semiconductor chip to a second side of the silicon interposer, wherein a number of electrical connections through the silicon interposer couple the first semiconductor chip to the second semiconductor;

forming a metal-to-semiconductor junction which couples to the first semiconductor chip on the first side of the silicon interposer, wherein forming the metal-to-semiconductor junction includes forming a Copper (Cu) and n or p-doped semiconductor junction wherein the semiconductor is selected from Bismuth Telluride (Bi_2Te_3), Lead Telluride (PbTe), and Silicon Germanium (SiGe); and

passing current through the metal-to-semiconductor junction in a direction such that a Peltier cooling effect occurs adjacent to the first semiconductor chip.

CONCLUSION

Claims 1-46 have been canceled. Claims 47-82 are therefor now pending. The Examiner is invited to contact the below-signed attorney with any questions regarding the present application.

Respectfully Submitted,

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Date of Deposit: June 26 , 2003
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